CLAIMS

1. An IC structure comprising:

a plurality of metal features provided on a substrate, said plurality of metal features including at least two substantially parallel adjacent metal lines having a speed sensitive pathway, each one of said metal lines having a separation S_{met} from the nearest of the other metal features; and

an enhanced metal line feature provided along at least one of said metal lines, said enhanced metal line having a first control spacing $DRCgap_1$ between said metal lines, and a second control spacing $DRCgap_2$ between said metal lines along said speed sensitive pathway, wherein $DRCgap_2 > DRCgap_1$.

2. The IC structure of claim 1 wherein $DRCgap_1 \geq S_{met}$.

3. The IC structure of claim 1 wherein change from the first control spacing $DRCgap_1$ to the second control spacing $DRCgap_2$ is incremental.

4. The IC structure of claim 1 wherein at an end of said speed sensitive pathway said enhanced metal line feature is decreased from $DRCgap_2$ to $DRCgap_1$.

5. The IC structure of claim 1 wherein said plurality of metal features further includes dummy metal features.

6. The IC structure of claim 1 further comprising a dielectric layer having a thickness of T_{idl} over said metal features.

7. The IC structure of claim 1 wherein $DRCgap_2$ is defined between $DRCgap_1$ and a maximum space that can be readily filled with an intermetal dielectric layer without negatively impacting Werner Fill processing.

8. The IC structure of claim 1 further comprising a guard ring circumscribing said metal features, said guard ring having said separation S_{met} to the nearest metal feature parallel thereto.

9. The IC structure of claim 1 wherein said plurality of metal features on said substrate includes dummy metal features, each having a width W_{met} and being situated in the separation between said metal features to provide said separation S_{met}.

10. The IC structure of claim 1 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, said plurality of metal features on said substrate includes dummy metal features, each having a width W_{met} and being situated in the separation between said metal features to provide said separation S_{met}, wherein:

S_{met} is not greater than $(1.4(n+1)T_{idl})+(n)W_{met})$ or twice T_{idl}; and

n is a maximized whole number not greater than $(S_{met} - 1.4T_{idl})/(1.4T_{idl} + W_{met})$.

11. The IC structure of claim 1 wherein at least one of said plurality of metal features is diagonally spaced from a nearest portion of another one of said plurality of metal features by a distance that is equal to $\sqrt{2}\, S_{met}$.

12. The IC structure of claim 1 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein a maximum spacing between nearest diagonally spaced points on said metal lines is less than or equal to about twice the thickness T_{idl} of the dielectric layer.

13. The IC structure of claim 1 wherein a minimum width of said metal features and a minimum spacing between closest parallel metal features are about equal, except along said speed sensitive pathway.

14. The IC structure of claim 1 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein said thickness of T_{idl} has a value of at least $(\sqrt{2}\, S_{met})/2$.

15. The IC structure of claim 1 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, and said plurality of metal features on said substrate includes dummy metal features, each having a width W_{met}, and being situated in the separation between said metal features to provide said separation S_{met}, wherein:

S_{met} is not greater than $(1.4(n+1)T_{idl})+(n)W_{met})$ or twice T_{idl};

n is a maximized whole number not greater than $(S_{met} - 1.4T_{idl})/(1.4T_{idl} + W_{met})$;

at least one of said plurality of metal features is diagonally spaced from the nearest portion of another one of said plurality of metal features by a distance that is equal to $\sqrt{2}\, S_{met}$; and

said thickness of T_{idl} has a value of at least $(\sqrt{2}\, S_{met})/2$.

16. The method of claim 15 wherein a maximum spacing between nearest diagonally spaced points on said metal lines is less than or equal to about twice the thickness T_{idl} of said dielectric layer.

17. The method of claim 15 wherein a minimum width of said metal features and a minimum spacing between the closest parallel metal features are about equal, except along said speed sensitive pathway.

18. An IC structure comprising:

a plurality of metal features provided on a substrate, said plurality of metal features including at least one speed sensitive pathway, each one of said metal features having a separation S_{met} from the nearest of the other metal features; and

an enhanced metal line feature provided on said substrate, said enhanced metal line having a first control spacing $DRCgap_1$ between said metal features, and a second control spacing $DRCgap_2$ between said metal features along said at least one speed sensitive pathway, wherein $DRCgap_2 > DRCgap_1$.

19. The IC structure of claim 18 wherein $DRCgap_1 \geq S_{met}$

20. The IC structure of claim 18 wherein S_{met} is from about 0.11μm to about 0.25μm.

21. The IC structure of claim 18 wherein change from the first control spacing $DRCgap_1$ to the second control spacing $DRCgap_2$ is incremental.

22. The IC structure of claim 18 wherein change from the first control spacing $DRCgap_1$ to the second control spacing $DRCgap_2$ is immediate.

23. The IC structure of claim 18 wherein at an end of said at least one speed sensitive pathway said metal line feature is decreased from $DRCgap_2$ to $DRCgap_1$.

24. The IC structure of claim 18 wherein $DRCgap_2$ is defined between $DRCgap_1$ and a maximum space that can be readily filled with an intermetal dielectric layer without negatively impacting Werner Fill processing.

25. The IC structure of claim 18 wherein said at least one speed sensitive pathway extends greater than about 10μm.

26. The IC structure of claim 18 wherein said plurality of metal features includes dummy metal features.

27. The IC structure of claim 18 further comprising a dielectric layer having a thickness of T_{idl} over said metal features.

28. The IC structure of claim 18 further comprising a guard ring circumscribing said metal features.

29. The IC structure of claim 18 wherein said plurality of metal features on said substrate includes dummy metal features, each having a width W_{met} and being situated in the separation between said metal features to provide said separation S_{met}.

30. The IC structure of claim 18 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, said plurality of metal features on said substrate includes dummy metal features, each having a width W_{met} and being situated in the separation between said metal features to provide said separation S_{met}, wherein:

S_{met} is not greater than $(1.4(n+1)T_{idl})+(n)W_{met})$ or twice T_{idl}; and

n is a maximized whole number not greater than $(S_{met} - 1.4T_{idl})/(1.4T_{idl} + W_{met})$.

31. The IC structure of claim 18 wherein at least one of said plurality of metal features is diagonally spaced from a nearest portion of another one of said plurality of metal features by a distance that is equal to $\sqrt{2}\, S_{met}$.

32. The IC structure of claim 18 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein a maximum spacing between nearest diagonally spaced points on said metal lines is less than or equal to about twice the thickness T_{idl} of the dielectric layer.

33. The IC structure of claim 18 wherein a minimum width of said metal features and a minimum spacing between closest parallel metal features are about equal, except along said at least one speed sensitive pathway.

34. The IC structure of claim 18 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein said thickness of T_{idl} has a value of at least $(\sqrt{2}\ S_{met})/2$.

35. An IC structure comprising:

a plurality of metal lines provided on a substrate, at least two of said metal lines being substantially parallel and adjacent to each other having at least one speed sensitive pathway;

dummy metal features, each having a width W_{met}, provided in separations between said metal lines;

a standard spacing S_{met} provided between each metal line and the nearest of one of said dummy metal features; and

an enhanced metal line feature provided along said at least one speed sensitive pathway, said enhanced metal line feature having a first control spacing $DRCgap_1$ between said adjacent metal lines, and a second control spacing $DRCgap_2$ between said adjacent metal lines along said speed sensitive pathways, wherein $DRCgap_2 > DRCgap_1$.

36. The IC structure of claim 35 wherein $DRCgap_1 \geq S_{met}$, wherein S_{met} is from about 0.11μm to about 0.25μm.

37. The IC structure of claim 35 wherein change from the first control spacing $DRCgap_1$ to the second control spacing $DRCgap_2$ at ends of said at least one speed sensitive pathway is selected from the group consisting of incremental, immediate, and combination thereof.

38. The IC structure of claim 35 wherein $DRCgap_2$ is defined between $DRCgap_1$ and a maximum space that can be readily filled with an intermetal dielectric layer without negatively impacting Werner Fill processing.

39. The IC structure of claim 35 wherein said at least one speed sensitive pathway extends greater than about 10μm.

40. The IC structure of claim 35 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein said metal features have a substantially equal thickness T_{met} and a width $\geq W_{met}$.

41. The IC structure of claim 35 further comprising a guard ring circumscribing said metal features, said guard ring having said separation S_{met} to the nearest metal feature parallel thereto.

42. The IC structure of claim 35 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein:

S_{met} is not greater than $(1.4(n+1)T_{idl})+(n)W_{met})$ or twice T_{idl}; and

n is a maximized whole number not greater than $(S_{met} -1.4T_{idl})/(1.4T_{idl} +W_{met})$.

43. The IC structure of claim 35 wherein at least one of said plurality of metal features is diagonally spaced from a nearest portion of another one of said plurality of metal features by a distance that is equal to $\sqrt{2}\ S_{met}$.

44. The IC structure of claim 35 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein a maximum spacing between nearest diagonally spaced points on said metal lines is less than or equal to about twice the thickness T_{idl} of the dielectric layer.

45. The IC structure of claim 35 wherein a minimum width of said metal features and a minimum spacing between closest parallel metal features are about equal, except along said speed sensitive pathway.

46. The IC structure of claim 35 further comprising a dielectric layer having a thickness of T_{idl} over said metal features, wherein said thickness of T_{idl} has a value of at least $(\sqrt{2}\ S_{met})/2$.